SM

Notice of Allowability	Application No. 10/773,909	Applicant(s) FUNAKI, TOSHIHIKO	
	Examiner son t. dinh	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ The drawings filed on *05 February 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/5/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *East search history*.

Son T. Dinh
Primary Examiner

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The prior art of record fail to teach or suggest a data writing method of a nonvolatile semiconductor memory device to reprogrammable nonvolatile semiconductor memory for storing N (N k 3) level of multilevel data by repeating a verification cycle of a write operation, a verify-read operation, and nonvolatile compare operation until write threshold level to memory cell exceeds a write level corresponding to an expected level, comprising the steps of: invalidating a verification result of a memory cell where a Nth threshold level) as an expected level by semiconductor which is a highest level is to be written mandatorily setting the verification result to "FAIL" until completion of writing to a memory cell where (N-1)th and lower threshold level, validating a verification result of the memory cell where the Nth level is to be written after reaching the (N-1)th write level (claim 1); a compare circuit for comparing data decoded by the decoder with the expected level data retained in the data register and outputting a verification result; a selection circuit for selecting between an output from the compare circuit and an output for mandatorily setting a verification result to "FAIL", and outputting a selected one as a verification result; and a selection signal generating circuit for outputting to the selection circuit a control signal for mandatorily setting a verification result of a memory cell where a Nth threshold level which is a highest level is to be written as an expected level to "FAIL" until completion of writing to a memory cell where a (N-1)th and lower threshold level is to be written as an expected level and validating a where the Nth level is verification result of the memory to be written after

reaching the (N-1)th write level, and outputting to the power unit a control signal for switching a first word line word line voltage for verification between the voltage in writing the (N-1)th and lower level and the second word line voltage in writing the Nth level; and an array of nonvolatile semiconductor memory cells for 40 storing one (N k 3) level data by repeating a verification setting a word line voltage supplied for the verify-reading in verification of the (N-1)th and word line voltage; and lower level data first setting a word line voltage supplied for the verify-reading in verification of the Nth level data) a compare circuit for comparing data decoded by the decoder with the expected level data retained in the data register to a second word line voltage which is higher than the first word line voltage .cycle of a write operation, a verify-read operation, and a compare operation until a write threshold level to nonvolatile semiconductor memory an expected level. (claim 6); and a method of data writing comprising the steps of setting a word line voltage supplied for the verify-reading in verification of the (N-1)th and word line voltage; and lower level data first setting a word line voltage supplied for the verify-reading in verification of the Nth level data to a second word line voltage which is higher than the first word line voltage (claim 12); a memory device comprising a compare circuit for comparing data decoded by the decoder with the expected level data retained in the data register and outputting a verification result; and a selection signal generating circuit for outputting to the power unit a control signal f or switching a word line voltage for verification between the first word line voltage in writing the (N-1)th and lower level and the second word line voltage writing the Nth level; and an array of nonvolatile semiconductor memory cells for storing one of N level data by repeating a verification

cycle of a write operation, a verify-read operation, and a compare operation until write threshold level to a nonvolatile semiconductor memory cell exceeds a write level corresponding to an expected level (claim 18).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-1868.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
April 16, 2005

Son T. Dinh